REMARKS

Claims 1-15 are currently pending in this application, with Claims 1, 12, and 14 being the only independent claims.

Examiner Grant is thanked for indicating that Claims 12 and 13 are allowed, and that Claims 3-7, 10, 11, and 15 would be allowable if rewritten in independent form. However, Claims 1, 2, 8, 9, and 14 remain rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,153,605 to *Ohara et al.*

Thus, reconsideration of the rejections of Claims 1, 2, 8, 9, and 14 is requested in view of the following remarks.

Rejection of Claim 1

One aspect of the claimed invention is defined by Claim 1 and is generally directed to an image processing apparatus having, among other features, a first processor which processes image data in correspondence to a first operation, a second processor which processes image data in correspondence to a second operation, and a memory shared by the first and the second processor.

Ohara et al. does not disclose both a first processor which processes image data in correspondence to a first operation and a second processor which processes image data in correspondence to a second operation together with the other claimed features defined by Claim 1.

On page two of the Official Action it is proposed that *Ohara et al.* shows a calculation circuit 25 and a correction data memory 23, and that such disclose the above-noted first and second processors defined by Claim 1. However, the portions of *Ohara et al.* describing the correction data memory 23 and the calculation circuit

25 do not support this proposition that both the correction data memory 23 and the calculation circuit 25 are image processors as defined by Claim 1. Specifically, it seems that the correction data memory 23 is not an image processor as defined by Claim 1, but rather a memory for storing density correction data corresponding to the variations of the respective heating elements R1 to Rn (column 5, line 67 to column 7, line 1). For example, in column 7, lines 35-44 (emphasis added) of *Ohara et al.*, it is stated that "the density correction data memory 23 stores the density correction data corresponding to the variations of the resistances of the respective heating elements R1 to Rn. The image signal corresponding to the first address ... is led from the data memory 10 to the calculation circuit 25, and at the same time the density correction data corresponding thereto is led from the density correction data memory 23 to the same calculation circuit 25. The calculation circuit 25 processes the inputted image signal and density correction data so as to produce image data corrected in correspondence with the variations of the resistances of the respective heating elements R1 to Rn." Further, in column 8, lines 14-21 (emphasis added) of *Ohara et al.*, it is stated that "the data memory 10 supplies the corresponding image signal to the calculation circuit 25 and the density correction data memory 23 supplies the corresponding density correction data to the same calculation circuit 25, whereby the calculation circuit 25 produces the corrected image data which are in turn supplied to the density data comparing circuit 14."

Ohara et al. does not disclose that the correction data memory 23 processes image data. The correction data memory 23 stores density correction data for use by the calculation circuit 25, and does not process image data as defined by Claim 1. For at least these reasons, *Ohara et al.* does not disclose a first processor which

processes image data in correspondence to a first operation and a second processor which processes image data in correspondence to a second operation as defined by Claim 1.

As an aside, it should be noted that on the middle of page three of the Official Action the correction data memory 23 is identified as being an image processor, and that on page two of the Official Action the correction data memory 23 is instead identified as being "a memory." It is respectfully requested that the next Official Action clarify the position being taken regarding the function of the correction data memory 23.

Ohara et al. also fails to disclose the feature directed to a memory that is shared by a first and a second processor as defined by Claim 1.

On page two of the Official Action, it is proposed that the shift register 16 and the latch circuit 17 in *Ohara et al.* is a memory shared by the correction data memory 23 and the calculation circuit 25 and that this discloses a memory shared by a first and a second processor as defined by Claim 1.

This proposition is not accurate at least for the reasons stated above, and because the latch circuit 17 and the shift register 16 do not serve as a memory for the correction data memory 23 and the calculation circuit 25. As can be seen in Figs. 3 and 7, a comparing circuit 14 is positioned between the correction data memory 23 and the calculation circuit 25. The density data comparing circuit 14 receives density correction data from the density correction data memory 23 (column 6, lines 37-42) and corrected image data from the calculation circuit 25, and outputs control data [0] or [1] to the shift register 16 (column 7, lines 64-67). This process is further described in *Ohara et al.* at column 6, lines 45-47(emphasis added), where it

is stated that "the density data comparing circuit 14 outputs a control data [1] to a shift register 16," and at column 6, lines 59-61(emphasis added) where it is stated that "the density data comparing circuit 14 supplies the control data [0] or [1] to the shift register 16." Further, in column 6, lines 63-67 (emphasis added) of *Ohara et al.*, it is stated that "the shift register 16 having n stages successively receives the control data [0] or [1] corresponding to the first to nth addresses in the first time on the first energization and supplies them to a latch circuit 17."

Nowhere does *Ohara et al.* disclose that the calculation circuit 25 and the correction data memory 23 use the shift register 16 or the latch circuit 17 as a memory, but rather that the shift register 16 or the latch circuit 17 receive output data from the comparing circuit 14. Should this rejection be maintained, it is respectfully requested that the Official Action more specifically explain how the shift register 16 or the latch circuit 17 described in *Ohara et al.* disclose a memory shared by a first and a second processor as defined by Claim 1, together with the other claimed features, or that this rejection be withdrawn.

Rejection of Claim 14

Another aspect of the claimed invention is defined by Claim 14 and is generally directed to an image forming apparatus having, among other features, a first processor which generates predetermined pattern data for test print, a second processor which processes image data for a normal print, and a memory that is shared by the first and second processors.

On the bottom of page three of the Official Action it is proposed that in *Ohara et al.*, the first energization is a test print for printing a predetermined pattern data

and the second energizaton is a second operation for normal printing as defined by Claim 14. This proposal is not accurate for at least the following reasons.

Ohara et al. only discloses an energization means for preheating and an energization means for printing, neither of which are a processor for generating predetermined pattern data for a test print as defined by Claim 14. In the portion of *Ohara et al.* concerning the first energizing (column 5, lines 42-47), it is stated that "the first energization means that pre-heating is effected by supplying currents to the respective heating elements R1 to Rn in accordance with density correction data in the density correction data memory 23 which corresponds to the variations of the resistances of the respective heating elements R1 to Rn..." Nowhere is predetermined pattern data for a test print disclosed.

Also, as noted earlier with respect to Claim 1, *Ohara et al.* does not disclose a first processor and a second processor as defined by Claim 14 or a memory shared by a first and a second image processor.

Should this rejection of Clam 14 be maintained, it is respectfully requested that it be more specifically pointed out how *Ohara et al.* discloses a first processor which generates predetermined pattern data for a test print, thereby affording a reasonable opportunity to respond to the Official Action, or that this rejection be withdrawn.

Rejections of Claims 2, 8 and 9

Claims 2, 8 and 9 depend from Claim 1 and are therefore allowable at least for the reasons set forth earlier with respect to independent Claim 1.

Conclusion

For at least the reasons stated above, it is requested that all the rejections be withdrawn, and that this application be allowed.

Should any questions arise in connection with this application, or should the Examiner feel that a telephone conference with the undersigned would be helpful in resolving any remaining issues pertaining to this application, the undersigned respectfully requests that he be contacted at the number indicated below.

Respectfully submitted,

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